Microelectronics Lab Report 3

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1 Overview

The following is a summary of the experiment I performed on March 26, where I constructed a number of basic circuits implementing diodes. I did this experiment on my own, five days after my peers did it, because I was ill with a viral flu on March 21. This illness led to pericarditis, and this lab report was not completed until late April.

2 Prelab Exercise 8

Prelab Exercise 8 described two circuits and asked me to describe their behaviour.

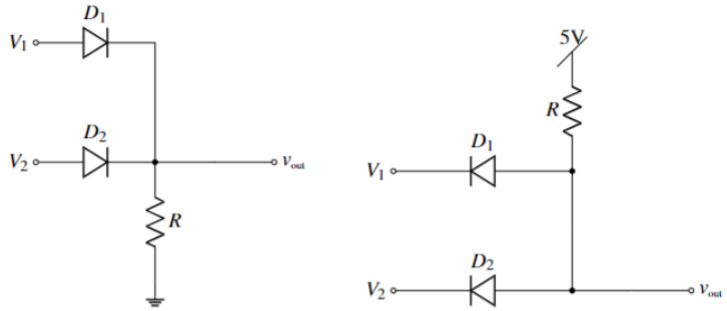

Figure 1. The circuits from Prelab Exercise 8.

The way that diodes should be analyzed is by assuming that they are in reverse bias and then switching them to forward bias in order of their voltage drop magnitude. As such, only the diode connected to the highest input voltage will be in forward bias in the left circuit, and only the diode connected to the lowest input voltage will be in forward bias in the right circuit.

The output of both of these circuits will be determined by the diode in the circuit that is in forward bias. 1N914 diodes have a forward voltage drop (VF) of 655 mV. As such, I know that the output of both circuits will be offset from the relevant input voltage by 655 mV.

V_1 (V)	V_2 (V)	Expected v_{out} (V)
3	2	2.345
3	2.8	2.345
3	3.2	2.545
3	4	3.345

Table 1. Predicted values of v_{out} for the left circuit from Prelab Exercise 8.

V_1 (V)	V_2 (V)	Expected v_{out} (V)
3	2	2.655
3	2.8	3.455
3	3.2	3.655
3	4	3.655

Table 2. Predicted values of v_{out} for the right circuit from Prelab Exercise 8.

3 Prelab Exercise 9

Prelab Exercise 9 described a circuit and asked me to describe its behaviour when v_{in} is a 1 kHz sinusoid with zero voltage offset, with a zero-to-peak amplitude of 2 V.

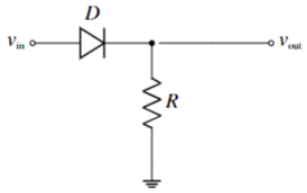

Figure 2. The circuit from Prelab Exercise 9.

This circuit is a halfwave rectifier. When $v_{in} < VF$, the diode will be in reverse bias against the ground voltage and v_{out} will be 0. When $v_{in} > VF$, $v_{out} = v_{in} - VF$.

When v_{in} is a 1 kHz sinusoid with zero voltage offset, the diode in this circuit is always in reverse bias when v_in is negative and usually in forward bias when v_in is positive. As a result, v_out recreates the top half of the sine wave at the same frequency and phase, peaking at 1.345 V.

4 Prelab Exercise 10

Prelab Exercise 10 described a circuit and asked me to describe its behaviour when v_{in} is a sinusoid with zero voltage offset and a zero-to-peak amplitude of 2 V.

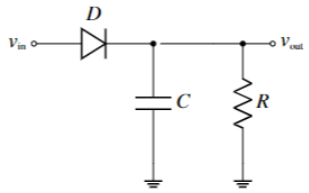

Figure 3. The circuit from Prelab Exercise 10.

This circuit is an envelope detector. As v_in increases, the capacitor is charged, until it reaches a maximum voltage of 1.345 V. The capacitor will then drive v_{out} as v_{in} decreases, then will keep driving v_{out} until $v_{in} = v_{out}$.

At low frequencies, this will produce no noticable effect, and this circuit will behave exactly like the halfwave rectifier in Prelab Exercise 9. As the frequency of the input (and, by extension, the output) increases, v_{out} will rise sinusoidally and fall linearly. As the frequency of the input approaches infinity, v_{out} approaches 1.345 V.

5 Prelab Exercise 11

Prelab Exercise 11 described a circuit and asked me to describe its behaviour when v_{in} is a 1 kHz sinusoid with zero voltage offset, with a zero-to-peak amplitude of 3 V.

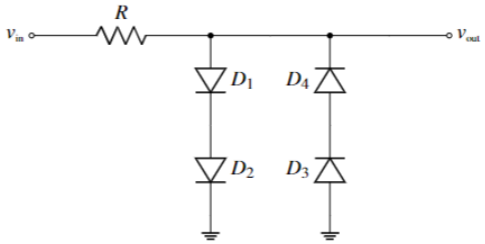

Figure 4. The circuit from Prelab Exercise 11.

This circuit is a combined voltage limiter and regulator. Since 1N914 diodes have a forward voltage drop (VF) of 655 mV, and since there are two 1N914 diodes in each leg of the circuit, the output voltage of this circuit will be constrained to be between -1.31 V and 1.31 V.

The output of this circuit, when fed a 3 V zero-to-peak signal, will resemble a squarewave: a near-flat moment at -1.31 V, a steep diagonal climb, another near-flat moment at 1.31 V, and a steep diagonal drop.

6 Prelab Exercise 12

Prelab Exercise 12 described a circuit and asked me to describe its behaviour when v_{in} is a 1 kHz sinusoid with a 1 V offset, with a zero-to-peak amplitude of 3 V.

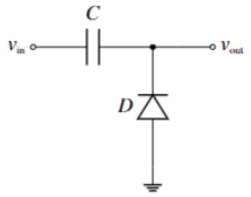

Figure 5. The circuit from Prelab Exercise 12.

This circuit is a clamped capacitor, also known as a DC restorer or DC restorator. v_{out} is constrained to never be less than $-VF$. The capacitor allows the circuit to approximate the initial signal, at the same maximum voltage and frequency. Since v_{in} is a 1 kHz sinewave from -2 V to 4 V, v_{out} will be a 1 kHz sinewave from -0.655 V to 4 V.

7 Procedure 1

Procedure 1 asked me to construct the circuits detailed in Figure 1 and to test several inputs of V2 while holding V1 constant at 3 V.

V_1 (V)	V_2 (V)	Measured v_{out} (V)
3	2	2.34
3	2.5	2.34
3	3	2.37
3	3.5	2.82
3	4	3.33

Table 3. Measured values of v_{out} for the left circuit detailed in Figure 1.

V_1 (V)	V_2 (V)	Measured v_{out} (V)
3	2	2.65
3	2.5	3.14
3	3	3.60
3	3.5	3.62
3	4	3.63

Table 4. Measured values of v_{out} for the right circuit detailed in Figure 1.

8 Procedure 2

Procedure 2 asked me to construct the circuit detailed in Figure 2 and to feed it a 1 kHz sinusoid with zero voltage offset with a zero-to-peak amplitude of 2 V, to see whether my prediction was accurate.

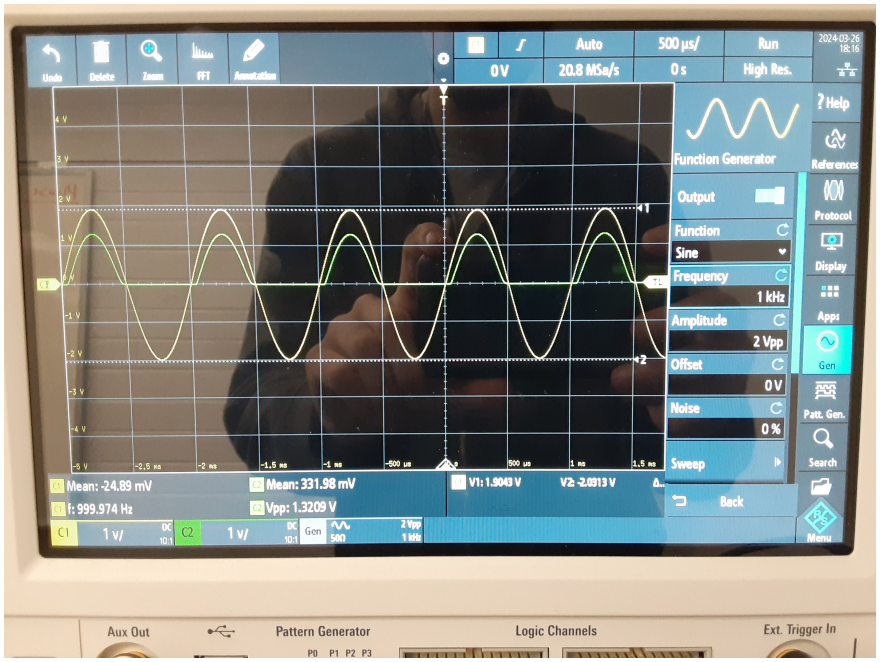

Figure 6. Behaviour of the circuit from Prelab Exercise 9. v_{in} is yellow and v_{out} is green.

The circuit behaves almost exactly as predicted. The maximum value reached by the output is 1.32 V, which is 0.68 V below the input. This is slightly larger than the predicted 0.655 V. This is likely caused by nonlinear characteristics of the diode. More surprisingly, when the diode is in reverse bias, the output stays at exactly 0 V instead of falling to -0.655 V as predicted.

9 Procedure 3

Procedure 3 asked me to construct the circuit detailed in Figure 3 and to feed it a sinusoid with zero voltage offset and a zero-to-peak amplitude of 2 V, to see whether my prediction was accurate.

At first, I used the same input signal as the previous circuit, and, as predicted, the result was exactly the same. 1 kHz was below the cutoff frequency of the circuit, and the capacitor was able to charge and discharge as quickly as the input voltage changed.

Next, I increased the frequency to 10 kHz. The output was similar to what I predicted, but much less linear. The peak-to-peak voltage is 1.43 V, which is slightly closer to the predicted 2 V.

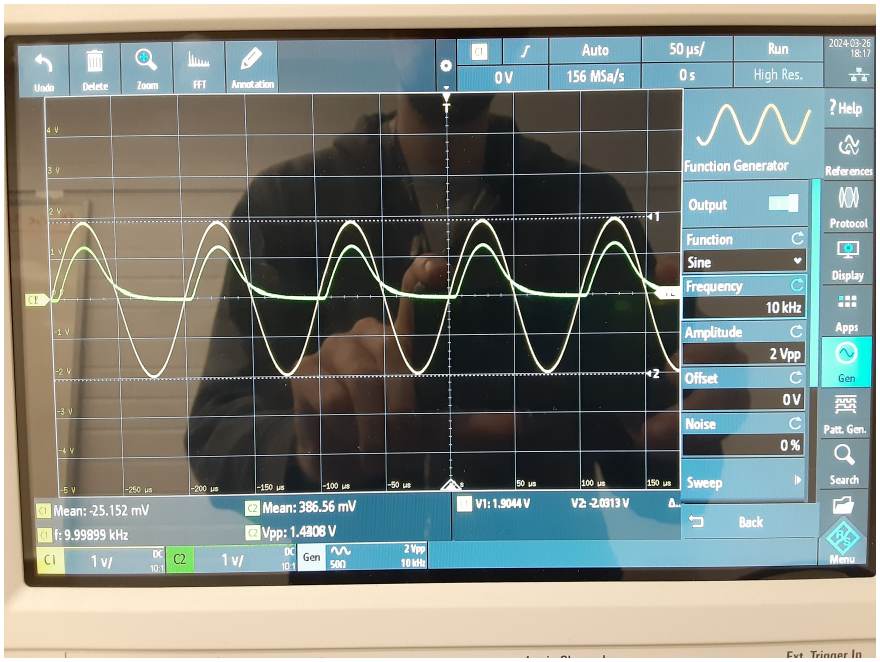

Figure 7. Behaviour of the circuit from Prelab Exercise 10 given a 10 kHz sinusoidal input. v_{in} is yellow and v_{out} is green.

I increased the frequency to 100 kHz. The result looked mush more similar to the predicted output, with a sinusoidal rise and linear fall. Curiously, while the capacitor is charging, the waveform of v_{in} is visibly deformed.

Figure 8. Behaviour of the circuit from Prelab Exercise 10 given a 100 kHz sinusoidal input. v_{in} is yellow and v_{out} is green.

10 Procedure 4

Procedure 4 asked me to construct the circuit detailed in Figure 4 and to feed it a 1 kHz sinusoid with zero voltage offset, to see whether my prediction was accurate.

At 2 V peak-to-peak, the limiter's output was exactly the same as its input. This was not surprising, as a 2 V peak-to-peak sinewave goes from -1 V to 1 V and the limiter's predicted cutoff voltages are -1.31 V and 1.31 V.

Figure 9. Behaviour of the circuit from Prelab Exercise 11 given a 2 V peak-to-peak sinusoidal input. v_{in} is yellow and v_{out} is green, but at this voltage they are the same.

I raised the voltage of the signal generator as high as it would go and the limiter began displaying more interesting output. Here, the output voltage ranges from -1.26 V to positive 1.26 V, just below what I predicted.

Figure 10. Behaviour of the circuit from Prelab Exercise 11 given a 5 V peak-to-peak sinusoidal input. v_{in} is yellow and v_{out} is green.

11 Procedure 5

Procedure 5 asked me to construct the circuit detailed in Figure 5, to ensure that my prediction was accurate. As predicted, vout was a 1 kHz sinewave from -0.655 V to 4 V.

12 Conclusion

The findings from this lab show that our models for estimating the outputs of elementary diode circuits are accurate. The output is usually slightly below what is expected. It is possible that this deficit is because of power dissipated through heat in the resistors of the circuit.